SM7100

MICROWAVE MATRIX

USER'S MANUAL

P/N: 82-0055-000
Released February 13, 2006

VXI Technology, Inc.

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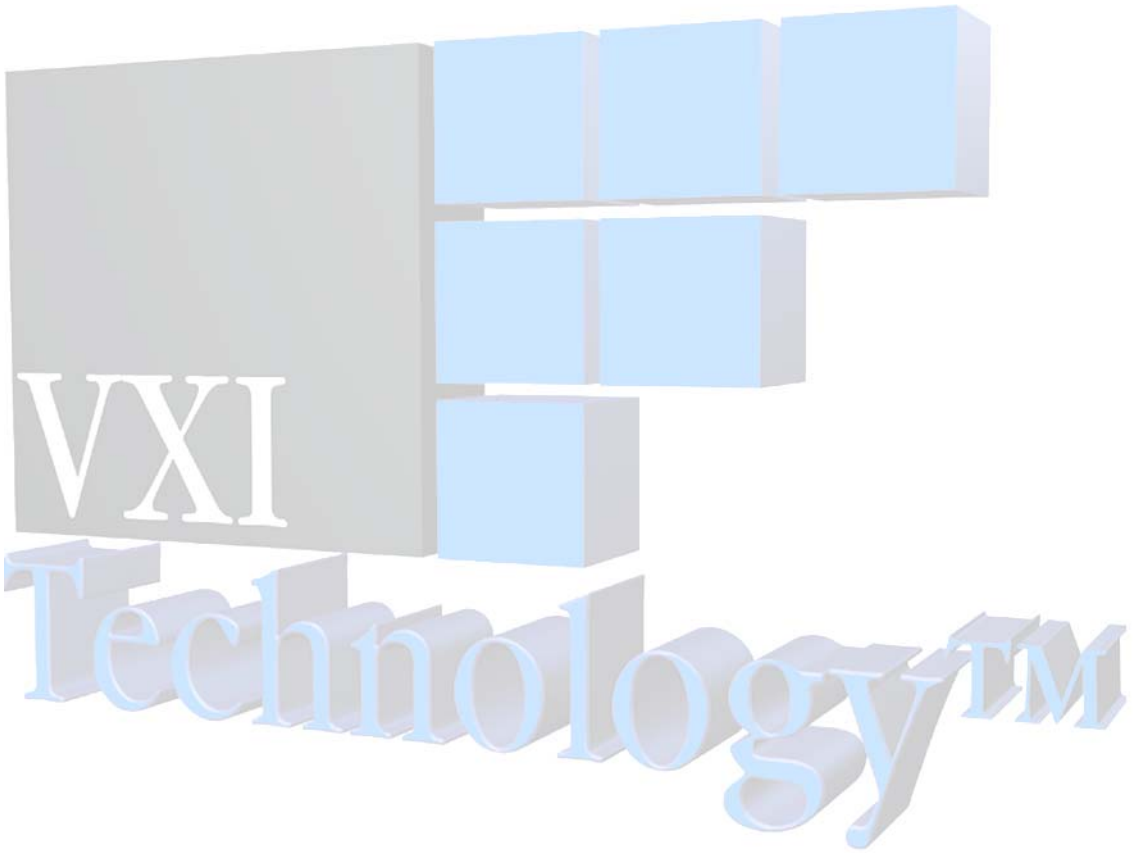
VXI
Technology™

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CERTIFICATION

VXI Technology, Inc. (VTI) certifies that this product met its published specifications at the time of shipment from the factory. VTI further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology (formerly National Bureau of Standards), to the extent allowed by that organization's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

The product referred to herein is warranted against defects in material and workmanship for a period of one year from the receipt date of the product at customer's facility. The sole and exclusive remedy for breach of any warranty concerning these goods shall be repair or replacement of defective parts, or a refund of the purchase price, to be determined at the option of VTI.

For warranty service or repair, this product must be returned to a VXI Technology authorized service center. The product shall be shipped prepaid to VTI and VTI shall prepay all returns of the product to the buyer. However, the buyer shall pay all shipping charges, duties, and taxes for products returned to VTI from another country.

VTI warrants that its software and firmware designated by VTI for use with a product will execute its programming when properly installed on that product. VTI does not however warrant that the operation of the product, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The warranty shall not apply to defects resulting from improper or inadequate maintenance by the buyer, buyer-supplied products or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

VXI Technology, Inc. shall not be liable for injury to property other than the goods themselves. Other than the limited warranty stated above, VXI Technology, Inc. makes no other warranties, express or implied, with respect to the quality of product beyond the description of the goods on the face of the contract. VTI specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

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VXI Technology, Inc.
2031 Main Street
Irvine, CA 92614-6509 U.S.A.

DECLARATION OF CONFORMITY

Declaration of Conformity According to ISO/IEC Guide 22 and EN 45014

MANUFACTURER'S NAME	VXI Technology, Inc.
MANUFACTURER'S ADDRESS	2031 Main Street Irvine, California 92614-6509
PRODUCT NAME	Microwave Matrix
MODEL NUMBER(S)	SM7100
PRODUCT OPTIONS	All
PRODUCT CONFIGURATIONS	All

VXI Technology, Inc. declares that the aforementioned product conforms to the requirements of the Low Voltage Directive 73/23/EEC *and the* EMC Directive 89/366/EEC *(inclusive* 93/68/EEC*) and carries the "CE" mark accordingly. The product has been designed and manufactured according to the following specifications:*

SAFETY	EN61010 (2001)
EMC	EN61326 (1997 w/A1:98) Class A CISPR 22 (1997) Class A VCCI (April 2000) Class A ICES-003 Class A (ANSI C63.4 1992) AS/NZS 3548 (w/A1 & A2:97) Class A FCC Part 15 Subpart B Class A EN 61010-1:2001

The product was installed into a C-size VXI mainframe chassis and tested in a typical configuration.

I hereby declare that the aforementioned product has been designed to be in compliance with the relevant sections of the specifications listed above as well as complying with all essential requirements of the Low Voltage Directive.

February 2006

CE

Steve Mauga, QA Manager

GENERAL SAFETY INSTRUCTIONS

Review the following safety precautions to avoid bodily injury and/or damage to the product. These precautions must be observed during all phases of operation or service of this product. Failure to comply with these precautions, or with specific warnings elsewhere in this manual, violates safety standards of design, manufacture, and intended use of the product.

Service should only be performed by qualified personnel.

TERMS AND SYMBOLS

These terms may appear in this manual:

WARNING Indicates that a procedure or condition may cause bodily injury or death.

CAUTION Indicates that a procedure or condition could possibly cause damage to equipment or loss of data.

These symbols may appear on the product:

ATTENTION - Important safety instructions

Frame or chassis ground

Indicates that the product was manufactured after August 13, 2005. This mark is placed in accordance with *EN 50419, Marking of electrical and electronic equipment in accordance with Article 11(2) of Directive 2002/96/EC (WEEE).* End-of-life product can be returned to VTI by obtaining an RMA number. Fees for take-back and recycling will apply if not prohibited by national law.

WARNINGS

Follow these precautions to avoid injury or damage to the product:

Use Proper Power Cord To avoid hazard, only use the power cord specified for this product.

Use Proper Power Source To avoid electrical overload, electric shock, or fire hazard, do not use a power source that applies other than the specified voltage.

Use Proper Fuse To avoid fire hazard, only use the type and rating fuse specified for this product.

WARNINGS (CONT.)

Avoid Electric Shock

To avoid electric shock or fire hazard, do not operate this product with the covers removed. Do not connect or disconnect any cable, probes, test leads, etc. while they are connected to a voltage source. Remove all power and unplug unit before performing any service. ***Service should only be performed by qualified personnel.***

Ground the Product

This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground.

Operating Conditions

To avoid injury, electric shock or fire hazard:

- Do not operate in wet or damp conditions.
- Do not operate in an explosive atmosphere.
- Operate or store only in specified temperature range.
- Provide proper clearance for product ventilation to prevent overheating.
- DO NOT operate if you suspect there is any damage to this product. ***Product should be inspected or serviced only by qualified personnel.***

Improper Use

The operator of this instrument is advised that if the equipment is used in a manner not specified in this manual, the protection provided by the equipment may be impaired.
Conformity is checked by inspection.

SUPPORT RESOURCES

Support resources for this product are available on the Internet and at VXI Technology customer support centers.

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SECTION 1

INTRODUCTION

OVERVIEW

The SM7100 Microwave Matrix is a member of the VXI Technology SMIP *II*™ (*Switch Modularity Interface Platform*) family. It offers a modular design allowing custom switching configurations in a single chassis.

The SM7100 is a double-wide, C-size VXI module, which can support customized microwave switch configurations for many applications.

Using the SMIP *II* family for microwave switching, the user obtains the following benefits over other VXI microwave switch solutions:

Density: Up to eight (1x6) microwave relays can be housed in a double-wide VXIbus slot, saving a complete C-Size slot.

Weight: The miniature relay technology reduces the overall weight considerably. Where possible, ultralight cabling is used maintaining the total weight under five pounds.

PROGRAMMING

The SMIP *II* family of switch modules is programmed using direct register access for fast data throughput.

Automatic Scanning

A predefined sequence of channels can be programmed into an extensive scan list that can be incremented by a trigger. This approach relieves the host controller from having to tie up the VXIbus backplane when scanning.

Programmable Timing Delays

A delay can be programmed between relay closures to allow for settling times of other system resources. When used with triggers, a controlled synchronous switching system can easily be configured.

Safety Interrupt

This is a programmable fail-safe feature that allows all relays to open based upon the occurrence of a selected TTL backplane trigger. This allows signals to be removed from the unit under test if a system fail-safe occurs, such as inadvertent removal of a test adapter.

SM7100 SPECIFICATIONS

SM7000 SPECIFICATIONS			
MAXIMUM POWER HANDLING (CW)			
At 18 GHz	20 W, 100 W peak pulse		
SWITCHING TIME			
	< 15 ms		
RF IMPEDANCE			
	50 Ω		
FREQUENCY (GHz)	**dc – 3**	**3 – 18**	**18 – 20**
Isolation (dB min)	90	80	60
Insertion Loss (dB max)	1.0	2.8	3.0
VSWR	1.2:1	1.6:1	2.0:1
SWITCH LIFE			
	1,000,000 cycles per switch		
CONNECTORS			
	SMA		
POWER REQUIREMENTS			
	+5 V @ 0.30 A -5.2 V @ 0.10 A -2 V @ 0.10 A 160 mA current draw per relay closure at +24 V		
COOLING REQUIREMENTS			
	2.22 L/s		

SECTION 2

PREPARATION FOR USE

INTRODUCTION

When the SMIP is unpacked from its shipping carton, the contents should include the following items:

(1) SMIP VXIbus module
(1) SM7100 Microwave Matrix User's Manual (this manual)

All components should be immediately inspected for damage upon receipt of the unit.

Once the SMIP *II* is assessed to be in good condition, it may be installed into an appropriate C-size or D-size VXIbus chassis in any slot other than slot zero. The chassis should be checked to ensure that it is capable of providing adequate power and cooling for the SMIP *II*. Once the chassis is found adequate, the SMIP's logical address and the chassis' backplane jumpers should be configured prior to the SMIP's installation.

CALCULATING SYSTEM POWER AND COOLING REQUIREMENTS

It is imperative that the chassis provide adequate power and cooling for this module. Referring to the chassis operation manual, confirm that the power budget for the system (the chassis and all modules installed therein) is not exceeded and that the cooling system can provide adequate airflow at the specified backpressure.

It should be noted that if the chassis cannot provide adequate power to the module, the instrument may not perform to specification or possibly not operate at all. In addition, if adequate cooling is not provided, the reliability of the instrument will be jeopardized and permanent damage may occur. Damage found to have occurred due to inadequate cooling would also void the warranty of the module.

SETTING THE CHASSIS BACKPLANE JUMPERS

Please refer to the chassis operation manual for further details on setting the backplane jumpers.

SETTING THE LOGICAL ADDRESS

The logical address of the SMIP *II* is set by two rotary switches located on the top edge of the interface card, near the backplane connectors. Each switch is labeled with positions 0 through F. The switch closer to the front panel of the module is the least significant bit (**LSB** or "**Front**"), and the switch located towards the back of the module is the most significant bit (**MSB** or "**Back**"). To set the Logical Address (LA), simply rotate the pointer to the desired value. For example, to set the **LA** to **25**, first convert the decimal number to the hexadecimal value of **19**. Next, set the back switch to **1**, and the front switch to **9**. See Figure 2-1. Two examples are provided below:

Example 1

LA (decimal)	Divide by 16		MSB	LSB	
25	25 / 16	=	1	w/ 9 remaining	*Divide the decimal value by 16 to get the MSB and the LSB.*
		=	0001	1001	*The 1 is the MSB, and the remainder of 9 is the LSB.*
		=	1	9	*Convert to hexadecimal. Set the back switch to 1 and the front switch to 9.*

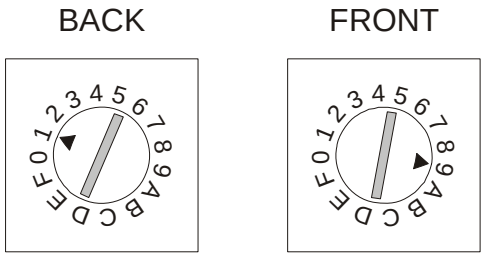


FIGURE 2-1: LOGICAL ADDRESS EXAMPLE 1

Example 2

LA (decimal)	Divide by 16		MSB	LSB	
200	200 / 16	=	12	w/ 8 remaining	*Divide by 16.*
		=	1100	1000	*Convert to MSB and LSB.*
		=	C	8	*Convert to hexadecimal. Set the back switch to C and the front switch to 8.*

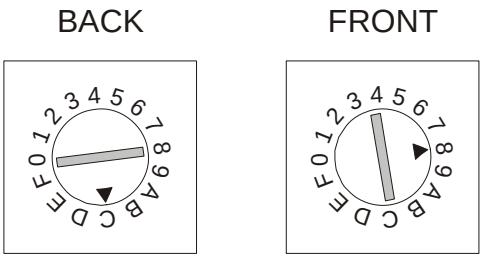


FIGURE 2-2: LOGICAL ADDRESS EXAMPLE 2

Here is another way of looking at the conversion:

LA = (back switch x 16) + front switch
LA = (1 x 16) + 9
LA = 16 + 9
LA = 25

Set the address switches to **FF** for dynamic configuration. Upon power-up, the resource manager will assign a logical address. See Section F - Dynamic Configuration in the *VXIbus Specification* for further information.

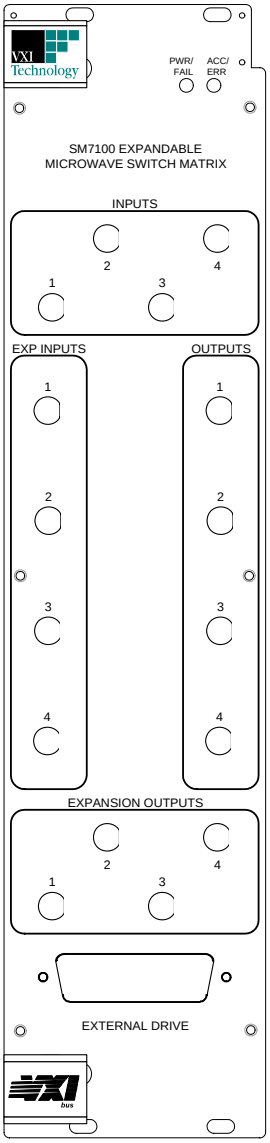
There is only one logical address per SMIP *II* base unit. Address assignments for individual modules are handled through the A24/A32 address space allocation.

SELECTING THE EXTENDED MEMORY SPACE

The Extended Memory Space of the SMIP *II* is set by a dip switch that is located on the bottom edge of the interface card. Position 1, located to the left on the dip switch, selects between A24 and A32 memory address space. In the UP position, the SMIP *II* will request A24 space. In the DOWN position, the SMIP *II* will request A32 space. (Position 2 is not currently used.) The selection of the address space should be based upon the memory allocation requirements of the system that the SMIP *II* module will be installed. The amount of memory allocated to the SMIP *II* module is independent of the address space selected.

SECTION 3

SWITCH CONFIGURATION



FRONT PANEL CONNECTION - SM7000

This section details the SM7100 schematics, relays, and pinouts. See Section 4, *Programming*, for information on relay addressing.

NOTE	Although ***pin numbers*** between the SM7000 and the HP equivalent differ, the ***signals*** remain in the same location. This makes it possible to use the same mating connector and cabling for either system. See Table 3-1 and Figure 3-3 for more information on connector J17.

FIGURE 3-1FIGURE 3-1 SM7100 FRONT PANEL

TABLE 3-1: SM7100 FRONT-PANEL EXTERNAL DRIVE CONNECTOR PIN ASSIGNMENTS – J17

SIGNAL	RELAY NUMBER	PIN NUMBER	HP EQUIVALENT
EXT 1	K49	J17-1	1
EXT 2	K51	J17-2	3
EXT 3	K53	J17-3	5
EXT 4	K55	J17-4	7
EXT 5	K57	J17-5	9
EXT 6	K59	J17-6	11
EXT 7	K61	J17-7	13
EXT 8	K63	J17-8	15
EXT 9	K65	J17-9	17
EXT 10	K67	J17-10	19
N/C	N/C	J17-11	21
+24V	+24V	J17-12	23
GND	GND	J17-13	25
EXT 14	K50	J17-14	2
EXT 15	K52	J17-15	4
EXT 16	K54	J17-16	6
EXT 17	K56	J17-17	8
EXT 18	K58	J17-18	10
EXT 19	K60	J17-19	12
EXT 20	K62	J17-20	14
EXT 21	K64	J17-21	16
EXT 22	K66	J17-22	18
EXT 23	K68	J17-23	20
+24V	+24V	J17-24	22
RETURN	GND	J17-25	24

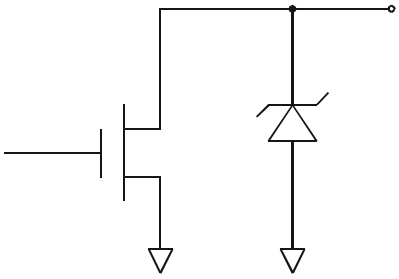


FIGURE 3-2: TYPICAL DRIVER OUTPUT

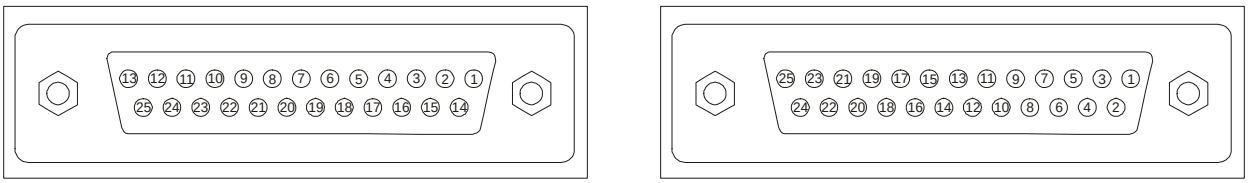


FIGURE 3-3: SM7100/HP EXTERNAL DRIVE PIN CROSS-REFERENCE

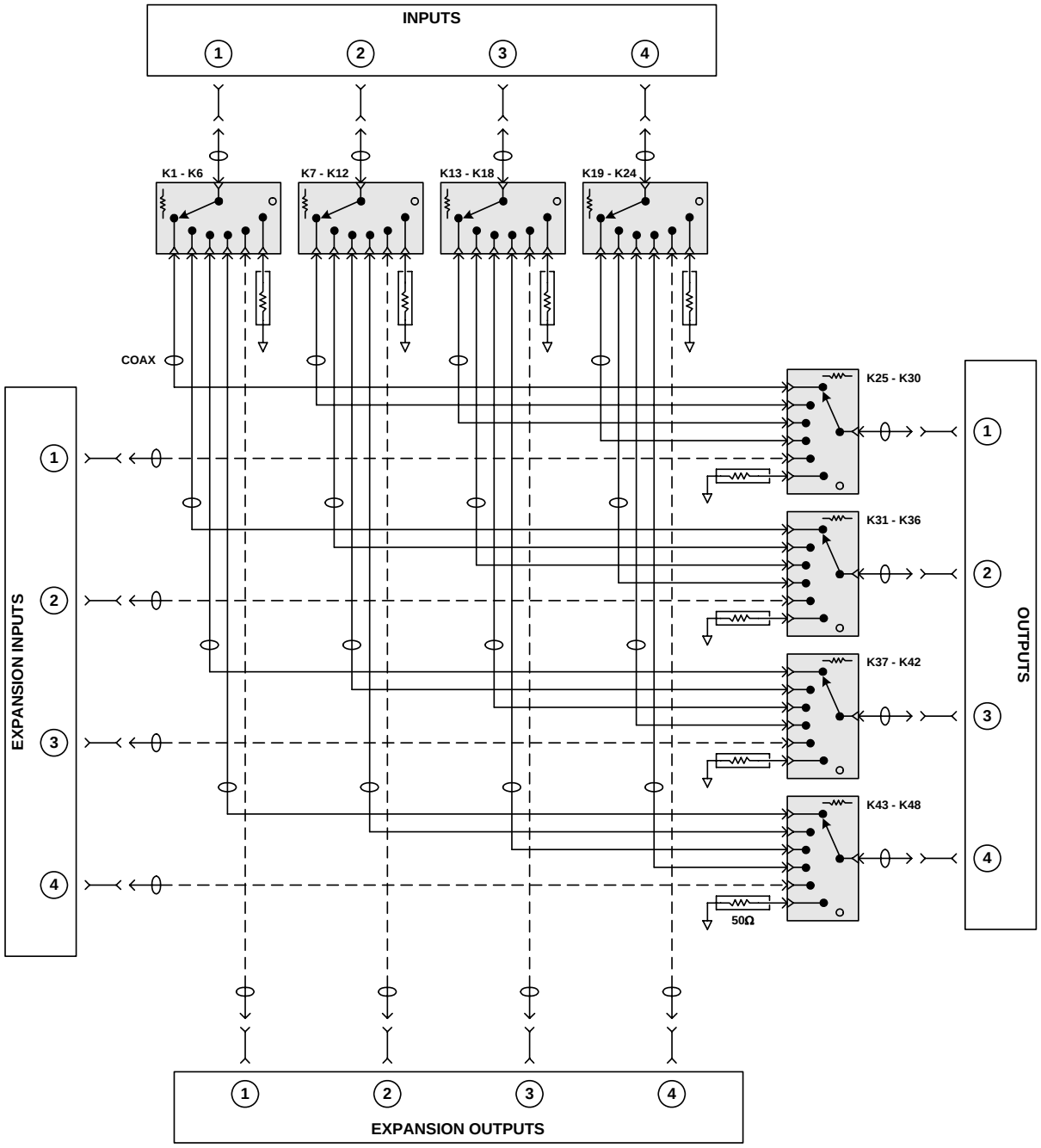


FIGURE 3-4: SM7100 MATRIX SCHEMATIC

TABLE 3-2: SM7100 RELAY REGISTER MAP

Offset (Hex)																
12																
10																
E																
C																
A																
8													K68	K67	K66	K65
6	K64	K63	K62	K61	K60	K59	K58	K57	K56	K55	K54	K53	K52	K51	K50	K49
4	K48	K47	K46	K45	K44	K43	K42	K41	K40	K39	K38	K37	K36	K35	K34	K33
2	K32	K31	K30	K29	K28	K27	K26	K25	K24	K23	K22	K21	K20	K19	K18	K17
0	K16	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1

SECTION 4

PROGRAMMING

REGISTER ACCESS

The SMIP *II* modules are VXIbus register-based devices for high-speed data transfers. Register-based programming is a series of **reads** and **writes** directly to the switch module registers. This eliminates the time for command parsing thus increasing speed.

ADDRESSING

The VTI switching modules utilize either the A24 or A32 space of the shared-memory architecture. To read or write to a module register, a register address needs to be specified. This is done by using the offset value (assigned by the resource manager) and multiplying it by 256 or 64 k to get the base address in A24 or A32 address space, respectively

A24 Base Address = Offset value * 0x0100 *(or 256)*

A32 Base Address = Offset value * 0x10000 *(or 65,536)*

The A24 or A32 offset value, assigned by the resource manager, can also be accessed by reading the A16 Offset Register. To address the A16 Offset Register use the following formula:

A16 Base Address = (Logical Address * 64) + 0xC000 *(or 49,152)*

then

A16 Offset Register Address = A16 Base Address + 6

See Table 4-1 for A16 Memory Map and A24/A32 address space allocation.

TABLE 4-1: SMIP *II* REGISTER MAP - A16

OFFSET	WRITE FUNCTION	READ FUNCTION
3E	Trace Advance	Board Busy
3C	Busy Trigger Control	Busy Trigger Control
3A	Trace RAM Control	Trace RAM Control
38	TTL Trigger Polarity	Reserved
36	Open Trigger Select	Reserved
34	Trace ADV Trigger Select	Reserved
32	Trace RAM Address LOW	Trace RAM Address LOW
30	Trace RAM Address HIGH	Trace RAM Address HIGH
2E	Trace RAM End LOW	Trace RAM End LOW
2C	Trace RAM End HIGH	Trace RAM End HIGH
2A	Trace RAM Start LOW	Trace RAM Start LOW
28	Trace RAM Start HIGH	Trace RAM Start HIGH
26	Module 5, 4 Used Address	Reserved
24	Module 3, 2 Used Address	Reserved
22	Module 1, 0 Used Address	Reserved
20	NVM Access Register	NVM Access Register
1E	Reserved	Subclass Register
1C	Interrupt Control	Interrupt Control
1A	Reserved	Interrupt Status
18	Reserved	Reserved
16	Reserved	Reserved
14	Reserved	Reserved
12	Reserved	Reserved
10	Reserved	Reserved
E	Reserved	Version Number
C	Reserved	Serial Number LOW
A	Reserved	Serial Number HIGH
8	Reserved	Reserved
6	Offset Register	Offset Register
4	Control Register	Status Register
2	Reserved	Device Type Register
0	LA Register	ID Register

DESCRIPTION OF REGISTERS - A16

The following describes the registers shown in the SMIP *II* Register Map for A16 address space.

ID Register (0x00) — Read Only		
D11-D0	Manufacturer's ID	VXI Technology, Inc., set to $F4B_{16}$
D13-D12	Address Space	A16/A24 = 00_2 A16/A32 = 01_2
D15-D14	Device Class	Extended register based device, set to 01_2

Logical Address Register (0x00) — Write Only		
D7-D0	Logical Address	Sets the new logical address in a dynamically configured module. When set for dynamic configuration (set to FF_{16}) a soft reset will not alter the configured logical address, while a hard reset will set the register back to FF_{16}.
D15-D8	Reserved	Writing to this range has no effect.

Device Type Register (0x02) — Read Only		
D11-D0	Model Code	Model 277, set to 115_{16}
D15-D12	Required Memory	2 Mbytes, set to 2_{16}, for A24 2 Mbytes, set to A_{16}, for A32

Status Register (0x04) — Read Only		
D15	A24/A32 Active	1 = indicates that A24/A32 memory space access is enabled 0 = indicates that A24/A32 memory space access is locked out
D14	MODID*	1 = indicates that the module is not selected by the MODID line 0 = indicates that the module is selected by the MODID line.
D13-D4	Reserved	These bits always read as $11,1111,1111_2$
D3	Ready	This bit always reads as 1_2
D2	Passed	This bit always reads as 1_2
D1-D0	Reserved	These bits always read as 11_2

Control Register (0x04) — Write Only		
D15	A24/A32 Enable	1 = write a 1 to this bit to enable A24/A32 memory access 0 = to disable access
D14-D2	Reserved	Writes to these bits have no effect.
D1	Sysfail Inhibit	Write a 1 to this bit to prevent the module from asserting the SYSFAIL* line.
D0	Reset	1 = write a 1 to this bit to force the module into a reset state 0 = write a 0 to release the reset state

Offset Register (0x06) — Read and Write		
D15-D0	A24/A32 Memory Offset	The value written to this 16-bit register, times 256, sets the base address of the A24 memory space used by the module. The value written to this 16-bit register, times 65,536, sets the base address of the A32 memory space used by the module. A read from this register reflects the previously written value. Because of the required memory size, bits D4 - D0 are disregarded on writes and always read back as 0. Upon receiving a hard reset, all bits in this register are set to 0. A soft reset does not affect the value in this register.

Reserved Register (0x0A) — Read Only		
D15-D0	Not Implemented	Always read back as $FFFF_{16}$

Reserved Register (0x0C) — Read Only		
D15-D0	Not Implemented	Always read back as $FFFF_{16}$

Version Number Register (0x0E) — Read Only		
D15-D8	Firmware Version Number	Not applicable, reads back as 00_{16}
D7-D4	Major Hardware Version Number	Depends on the specific hardware revision of the SMIP *II* interface board.
D3-D0	Minor Hardware Version Number	Depends on the specific hardware revision of the SMIP *II* interface board.

Interrupt Status Register (0x1A) — Read Only		
D15	Scan Function done	The latest scan list update is complete.
D14	Openbus Active Event true	The Openbus was activated by one or more programmed inputs. See description of the Openbus in the module register section.
D13-D9	Unused	Data written to these bits have no effect.
D8	Module Busy Complete	The programmed Busy signal from the module has timed out. This indicates that the relays actuated for that Busy cycle have settled and a measurement may take place.
D7-D0	Reserved	Always reads back as $FFFF_{16}$
Note: This status register may be used in a polled fashion rather than allowing the events above to generate an Interrupt. A read of this register will clear any active bits. Bits that are not set, or are about to be set are not affected by a read of this register.		

Interrupt Control Register (0x1C) — Read and Write		
D15	Scan Function done mask bit	0 = enabled 1 = disabled
D14	Openbus Active Event true mask bit	0 = enabled 1 = disabled
D13-D9	Unused	Data written to these bits has no effect
D8	Module Busy Complete	0 = enabled 1 = disabled
D7	IR ENA*	0 = writing a 0 to this bit enables interrupter capabilities 1 = writing a 1 to this bit disables interrupter capabilities
D6	IH ENA*	The module has no interrupt handler capability; therefore writing a 1 or 0 has no effect. A 1 is always read back for this bit.
D5-D3	Interrupter IRQ Line	The complement of the value programmed into these three bits reflects the selected IRQ line used by the module. A value of 011_2 would select IRQ4, a value of 000_2 would select IRQ7, and a value of 111_2 would disconnect the IRQ lines.
D2-D0	Handler IRQ Line	The module has no interrupt handler capability; therefore writing to these bits has no effect. A 111_2 is always read back for these bits.
Note that all bits in this register are set to 1 upon receipt of a hard or soft reset.		

Subclass Register (0x1E) — Read Only		
D15	VXIbus Extended Device	Always reads as 1.
D14-D0	Extended Memory Device	Always reads as $7FFD_{16}$

NVM Access Resister (0x20) — Read Only		
D15-D1	Unused	All Bits are always 1.
D0		Reads back the serial data stream from the selected SMIP *II* board. Note that only one SMIP *II* board may be read back at a time.

NVM Access Resister (0x20) — Write Only		
D15-D2	Unused	Data written to these bits have no effect.
D1		Serial clock for the switch module; should be a logic 1 when not used.
D0		Serial data input for the switch module; must be a logic 1 when not used.

Board X, Y Used Address Register (0x22, 0x24, 0x26) — Read and Write		
D15-D8		Sets the actual number of words of address space used by the relays on board's X.
D7-D0		Sets the actual number of words of address space used by the relays on board's Y.

Trace RAM Start High Register (0x28) — Read and Write		
D15-D4	Unused	Data written to these bits have no effect and always read back as 1.
D3-D0		Sets the four most significant bits of the starting address of the Trace RAM, allowing the available RAM to be divided into multiple traces.

Trace RAM Start Low Register (0x2A) — Read and Write		
D15-D0		Sets the 16 least significant bits of the starting address of the Trace RAM, allowing the available RAM to be divided into multiple traces.

Trace RAM End High Register (0x2C) — Read and Write		
D15-D4	Unused	Data written to these bits have no effect and always read back as 1.
D3-D0		Sets the four most significant bits of the ending address of the Trace RAM, allowing the available RAM to be divided into multiple traces.

Trace RAM End Low Register (0x2E) — Read and Write		
D15-D0		Sets the 16 least significant bits of the ending address of the Trace RAM, allowing the available RAM to be divided into multiple traces.

Trace RAM Address HIGH Register (0x30) — Read and Write		
D15-D4	Unused	Data written to these bits have no effect and always read back as 1.
D3-D0		Sets and reads back the four most significant bits of the current address of the Trace RAM, allowing the current trace RAM address to be queried and changed.

Trace RAM Address LOW Register (0x32) — Read and Write		
D15-D0		Sets and reads back the sixteen least significant bits of the current address of the Trace RAM, allowing the current trace RAM address to be queried and changed.

Trace Advance Trigger Select Register (0x34) —Write Only		
D15-D8		Sets the TTLTRIG line or lines, which are configured as outputs, and will toggle when Trace Advance condition occurs in the module. D15 corresponds to TTLTRIG7, D14 to TTLTRIG6, … and D8 to TTLTRIG0. Setting a bit to a 1 enables the trigger line, setting a bit to 0 disables the corresponding line. All bits are set to 0 when either a soft or a hard reset is received by the module.
D7-D0		Sets the TTLTRIG line or lines, which are configured as inputs, and will cause a Trace Advance event to occur in the module. D7 corresponds to TTLTRIG7, D6 to TTLTRIG6, … and D0 to TTLTRIG0. Setting a bit to a 1 enables the trigger line, setting a bit to 0 disables the corresponding line. All enabled TTLTRIG lines are OR'd together to allow more than one TTLTRIG line to cause a Trace Advance event to occur. All bits are set to 0 when the module receives either a soft or a hard reset.

Open Trigger Select Register (0x36) —Write Only		
D15-D8		Sets the TTLTRIG line or lines, which are configures as outputs, and will toggle when Relay Open condition occurs in the module. D15 corresponds to TTLTRIG7, D14 to TTLTRIG6, … and D8 to TTLTRIG0. Setting a bit to a 1 enables the trigger line, setting a bit to 0 disables the corresponding line. All bits are set to 0 when either a soft or a hard reset is received by the module.
D7-D0		Sets the TTLTRIG line or lines, which are configured as inputs, and will cause a Relay Open event to occur in the module. D7 corresponds to TTLTRIG7, D6 to TTLTRIG6, … and D0 to TTLTRIG0. Setting a bit to a 1 enables the trigger line, setting a bit to 0 disables the corresponding line. All enabled TTLTRIG lines are OR'd together to allow more than one TTLTRIG line to cause a Relay Open event to occur. All bits are set to 0 when the module receives either a soft or a hard reset.

TTL Trigger Polarity Register (0x38) —Write Only		
D15-D9	Unused	Data written to these bits have no effect.
D8	FAIL LED Control	0 = off 1 = on
D4	Board Busy Trigger Slope	0 acts on the falling edge, 1 acts on the rising edge.
D3	Relay Open Input Slope	0 acts on the falling edge, 1 acts on the rising edge.
D2	Relay Open Output Slope	0 sets the falling edge active, 1 sets the rising edge active.
D1	Trace Advance Input Slope	0 advances on the falling edge, 1 advances on the rising edge.
D0	Trace Advance Output Slope	0 sets the falling edge active, 1 sets the rising edge active.
Note: A hard or a soft reset sets D3 - D0 to 0.		

Trace RAM Control Register (0x3A) — Read and Write		
D15-D11	Unused	Data written to these bits have no effect.
D15-D10	Modules Installed	Set to 0 if the module is installed or set to a 1 if not installed. These bits are set to 0 at power on. By setting a 1, the SMIP *II* Interface PCB will generate DTACK for any read or write cycles to the memory space of the uninstalled plug-in module.
D9-D5	Unused	Data written to these bits have no effect.
D4	Modules used in trace mode	D9 is for module 5, D4 is for module 0. Set to 1 if the module is used in trace mode, set to 0 if not in trace mode.
D3-D2	Unused	Data written to these bits have no effect. The value written is read back.
D1	LOOP ENABLE	1 = Enabled, 0 = Disabled. If enabled, the trace resumes at the start of active RAM and continues from there. If disabled, the trace stops at the end of active RAM and clears the TRACE ENABLE bit.
D0	TRACE ENABLE	1 = enabled, 0 = disabled. If the LOOP ENABLE bit is set and the end of active trace RAM is reached, this bit will not be reset.

Busy Trigger Control Register (0x3C) — Read and Write		
D15-D8	TTLTRIG Select	Sets the TTLTRIG Line or Lines, which are configured as outputs, and will toggle at the de-assertion of a Board Busy condition sent by the plug-in modules. D15 corresponds to TTLTRIG7, D14 to TTLTRIG6, … and D8 to TTLTRIG0. Setting a bit to a 1 enables the trigger line, setting a bit to a 0 disables the corresponding line. All bits are set to 0 when either a soft or a hard reset is received by the module.
D7-D1	Unused	Data written to these bits have no effect. The value written is read back.
D0	Busy Trigger Enable	Enables the Board Busy signal received from the switch module to generate a trigger condition on the TTL Trigger Bus. Setting a bit to 1 enables the generation of a Trigger condition, setting a bit to a 0 disables the corresponding line. This bit is set to 0 when either a soft or a hard reset is received by the module.

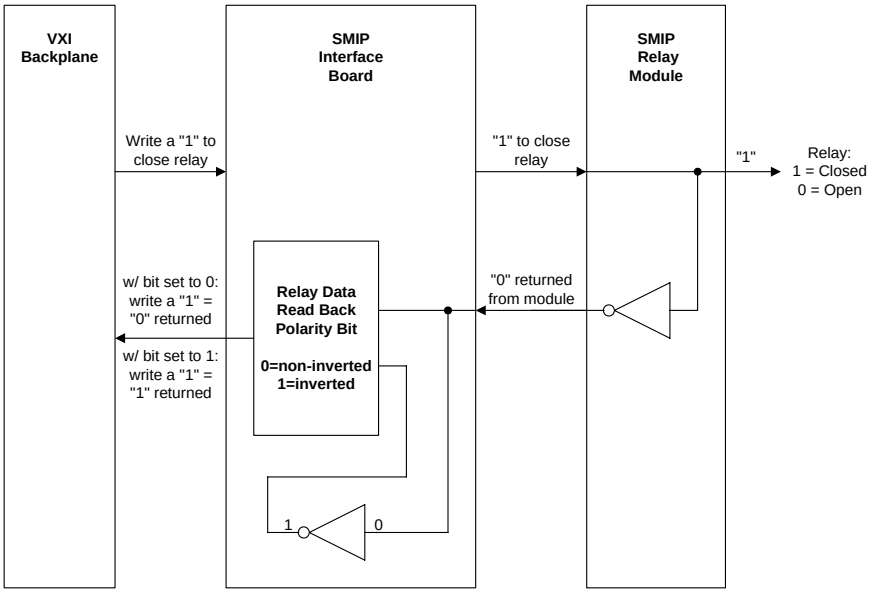
Trigger Advance Register (0x3E) — Write Only		
D15-D0	Unused	The act of writing to this location causes a Trace Advance event to occur in the module. The specific data written to these bits has no effect.

Board Busy Register (0x3E) — Read Only		
D15-D7	Unused	These bits always read back as 1.
D6		Indicates whether the SMIP *II* platform is a single or double wide. 0 = single wide 1 = double wide
D5-D1	Unused	Data written to these bits have no effect.
D0		A 0 read from this bit indicates the relays on the switch module have settled, a 1 indicates that the relays on the switch module are still changing state.

Reserved Registers — Read and Write		
D15-D0	Unused	Writing to these registers has no effect and will always read back as $FFFF_{16}$.

DESCRIPTION OF SMIP *II* MODULE REGISTERS - A24 / A32 - EXTENDED MEMORY

Each module is assigned 1 k (1024) bytes of memory as shown in the SMIP *II* Configuration/Relay Register Map for A24/A32 address space. The upper 512 bytes of memory space is used for module configuration registers. The following describes these registers.

<table>
<tr><th colspan="3">Control Register - Read and Write</th></tr>
<tr><td>ADDR</td><td colspan="2">Plug-In LA+0x200</td></tr>
<tr><td>D15-D10</td><td>Unused</td><td></td></tr>
<tr><td>D9</td><td>Relay Data Read Back Polarity Bit</td><td>0 = Normal polarity relay data is read back from this module
1 = Inverted polarity relay data is read back from this module
Pon state = 0
 

This bit may be used to invert the relay data read back from the plug-in module. Control, Delay, and Status Register read backs are not effected by this bit.</td></tr>
<tr><td>D8</td><td>ACFAILN Enable Bit</td><td>0 = ACFAILN is enabled to reset this module's relays
1 = ACFAILN is disabled from resetting this module's relays
Pon state = 0</td></tr>
</table>

Control Register - Read and Write (continued)		
D7	BBM/MBB Enable Bit	0 = BBM (Break-Before-Make) / MBB (Make-Before-Break) is disabled 1 = BBM/MBB operation is enabled Pon state = 0 ***NOTE: This bit should remain a 0 (disabled) for the SM7100.*** If this bit is set, the relays will be sequenced to effect proper BBM or MBB operation. If this bit is not set, the module will process the newly written relay data as immediate data, writing it directly to the relay driver ports. No BBM or MBB sequencing will take place. While this feature is enabled, the initial write to the module will start the delay timer running and begin the BBM or MBB operation. Since the relays are controlled by the 16-bit registers, only the effected 16 relays will perform the BBM/MBB operation. To overcome this fact, any subsequent writes to the module, during the initial delay timer time-out period, will be accepted and processed. In addition, the delay time will be reset and begin counting down again. Once the delay timer has timed-out (this indicates that the relays have settled into their BBM/MBB state), writes to the module will not be accepted and may result in a Bus Error depending on the value programmed into the delay timer. This is because the delay timer is reset at the end of the initial time-out and is used to time the final relay closure into their post BBM/MBB state. The module Busy signal will only complete once the final relay closure state is reached. If this bit is set and no value has been loaded into the Delay Register, the module will act as if this enable bit is not set and load all of the relay drivers with immediate data.
D6	BBM/MBB Select Bit	0 = BBM operation is selected 1 = MBB operation is selected Pon state = 0 ***NOTE: This bit should remain a 0 (BBM) for the SM7100.***
D5	Access LED Fail Bit	0 = non-active 1 = active Pon state = 0 Lights the Access LED red when activated.
D4	Relay Reset Enable Bit	0 = The Openbus and Front Panel Open signals are not enabled to reset the relays 1 = The Openbus or Front Panel Open signal may be selected to reset the relays Pon state = 0
D3	Relay Reset Select Bit	0 = Front Panel Open signal is selected to reset the relays 1 = The Openbus signal is selected to reset the relays Pon state = 0 Many plug-in modules may be programmed to be listeners on the Openbus.
D2	Openbus Out Enable Bit	0 = Disables the Front Panel Open signal from driving the Openbus signal 1 = Enables the Front Panel Open signal to drive the Openbus Pon state = 0.

Control Register - Read and Write (continued)		
D1	Front Panel Open Signal Polarity Bit	0 = Non-inverted Front Panel Open signal polarity 1 = Inverted Front Panel Open signal polarity Pon state = 0 Non-inverted: If set in pulse mode, the Front Panel Open signal will generate a reset pulse on a falling edge. If set in level mode, the Front Panel Open signal will generate a reset signal on a low input signal. Inverted: If set in pulse mode, the Front Panel Open signal will generate a reset pulse on a rising edge. If set in level mode, the Front Panel Open signal will generate a reset signal on a high input signal.
D0	Front Panel Open Signal Operation Select Bit	0 = Pulse mode 1 = Level mode Pon state = 0 Pulse mode: An edge seen at the Front Panel Open signal pin will generate a reset pulse that may be used to reset system relays. The pulse is of approximately 300 ns duration. Level mode: A level present on the Front Panel Open signal pin will generate a reset signal that may be used to reset system relays. This signal will remain active as long as the input is active. On the front panel of most SMIP *II* plug-in modules, there are two pins for access to the Front Panel Open signal of the module. These are the Front Panel Open signal pin and a ground reference pin. The purpose of the Front Panel Open signal is to allow user access to a configurable interlock feature that will reset all of the SMIP *II* system relays. The Front Panel Open signal may be used to reset the relays only on the module, which initiated the Front Panel Open signal fault condition. It also may be used to broadcast to all the other SMIP *II* plug-in modules installed in a SMIP *II* Interface Module via what is called the Openbus. Any plug-in module may be programmed to drive and/or listen to the Openbus. The Openbus signal may also be used to generate a wider chassis level fault signal via the TTL Trigger Bus (see the register definitions for A16 address space). The Front Panel Open signal is meant to be driven by either a switch closure or TTL/CMOS logic gate. It is pulled high on the module.

Delay Register - Read and Write		
ADDR	Plug-In LA+0x202	
D15-D0	Data Bus 16 Bit	This register is used to set the time that the plug-in module will hold the Board Busy signal active. The Board Busy signal is set every time the plug-in receives a Write to a relevant Relay Register memory space. The Board Busy signal will be removed at the end of the time out that is set by the value contained in this register. For each count loaded into this register, the Board Busy signal will be held active for 1 μs. The delay may be set from 0 to approximately 65 ms, thus accommodating a wide variation in test station requirements. The Board Busy signal may be monitored by the user, in either a polled or an interrupt fashion, and is to be used as an indication that the relays in the newly actuated path have settled. Alternatively, the Board Busy signal may also be used to drive the TTL Trigger Bus. See the Board Busy, Interrupt Control and Busy Trigger Control Register descriptions in the A16 address space.

Status Register - Read Only		
ADDR	Plug-In LA+0x204	
D15-D13	Hardware Revision Code	
D12-D1	Unused	
D0	Front Panel Open signal set by this module	0 = Indicates that the module's Front Panel Open signal was not activated by the user 1 = An indication that the module's Front Panel Open signal was activated as programmed by the user Pon state = 0 A read of this bit location will indicate whether the Front Panel Open signal was triggered from the front panel of the module. A read of this register clears this bit to 0.

DEVICE MEMORY MAP

RELAY REGISTER OFFSET

The Relay Register Offset is located within the A24/32 address space of the module. When you send data to the register, the relay register offset is added to the A24/A32 base address and module base address:

Relay Register Address = A24/A32 Base Address + Module Base Address + Register Offset

or

Relay Register Address = Module Relay Address + Register Offset

WRITING TO THE RELAYS

Each bit of a 16-bit register represents the state of the relay (1 = closed, 0 = open). To change the state of any relay, it is only necessary to write a 16-bit integer to the specified register with the new configuration:

Relay Register Address, **data**

For example:

- writing a data value of "0" to the register at offset "0" would open the first sixteen relays
- writing a data value of 65535 to the same register would close the first 16 relays
- writing a data value of 65534 to the same register would close all relays except K1, which would be open

NOTE	*Energize only one coil in a group of six at one time.*

PROGRAMMING

With the introduction of VISA, sending a command to a register-based device is as simple as sending a command to a message-based device. Whether the application is graphical or standard, sending commands to the register-based device is just as intuitive. The VISA template for transferring data to a register-based device, utilizing A32 extended memory space, is as follows:

```
viOut16 (Handle, VI_A32_SPACE, Offset, Data)
```

Handle is passed by reference whenever a VISA session to a particular device is opened.

VI_A32_SPACE is defined in the VISA header file. (VI_A16_SPACE and VI_A24_SPACE are also valid.)

Offset is determined from the memory map and is in decimal format.

Data is a 16-bit signed integer value representing the state of the relays.

The following example is for a SM5001, 80 channel SPST relay card utilizing A32 extended memory space. To close relays K1, K33 and K48 while leaving the other relays open, the following commands would be sent:

```
viOut16 (Handle, VI_A32_SPACE, 0, 1)       'closes relay 1
viOut16 (Handle, VI_A32_SPACE, 4, 32769)   'closes relay 33 and 48
```

VISA is the software architecture standard instituted by the VXI*plug&play* Alliance and is at a very high level of communication to a VXIbus device. The same philosophy and simplicity applies if the instrument is being programmed via lower level commands of an API (Application Programmer's Interface).

The device Relay Register Map is shown in the following table.

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